Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application

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***Abstract*—This paper presents a comprehensive review of step-up single-phase non-isolated inverters suitable for ac-module applications. In order to compare the most feasible solutions of the reviewed topologies, a benchmark is set. This benchmark is based on a typical ac-module application considering the requirements for the solar panels and the grid. The selected solutions are designed and simulated complying with the benchmark obtaining passive and semiconductor components ratings in order to perform a comparison in terms of size and cost. A discussion of the analyzed topologies regarding the obtained ratings as well as ground currents is presented. Recommendations for topological solutions complying with the application benchmark are provided**

***Index Terms*—AC-module, photovoltaic (PV), step-up inverter, transformerless.**

I. Introduction

THE interest in using renewable energies has grown significantly in the last years. In 2010, photovoltaic (PV) was the leading renewable energy technology in terms of capacity growth in Europe, with 13.3 GW installed, as a comparison to the 9.3 GW for wind power [1]. Within PV systems, power inverters are required to inject the PV power into the ac grid. In [2], a summary of the power configurations for PV systems is presented. Traditionally, centralized inverters have been used for solar farms. Currently, string and multistring inverters, as well as their bypass module and generation control circuit concept variations, are extensively used in utility-scale PV systems. In residential applications, most research is focused on the module-integrated converters, such as ac-module technology and dc–dc power optimizers [3], [4].

The ac module is composed of a grid-connected inverter (micro-inverter) attached to a PV module. One of the main advantages of these PV systems is the modularity, allowing an easy increase of the installed power. In addition, since the maximum power point tracking (MPPT) is implemented for each individual PV module, partial shading and panel mismatching are reduced, thus improving the energy harvesting capability.

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The main design challenges within the ac modules are the further improvements within efficiency as well as guaranteeing reliable operation throughout the module lifetime. In addition, the manufacturing costs of an individual module are relatively high, and therefore, mass production of these inverters would decrease the cost at the long term. This fact, together with the decreasing PV module prices [5] introduces an opportunity for ac modules to become more "plug and play" devices and thereby reducing the overall system costs.

Several topologies for ac-module application have been presented [6], [7]. Due to the high voltage boost required to interface the low output voltage of the PV module to the grid, the use of a transformer is widespread. In [8], a survey of commercial PV inverter topologies in terms of maximum efficiency, weight, and volume is presented. As a result, transformerless topologies are more efficient, lighter, less bulky, and less costly than the isolated inverters, independent if a low- or high-frequency transformer is utilized. However, a main concern to be addressed in non-isolated PV inverters is the grounding and the leakage ground currents through the solar panel parasitic capacitance [9].

In [10], the parallel-connected configuration of PV modules is analyzed. As in ac-module applications, the resulted array voltage is low and step-up high-efficiency converters are necessary. Therefore, the nonisolated high step-up dc–dc converters that solve the practical implementation problems of a high gain boost converter are reviewed. Furthermore, the authors introduce soft-switched coupled inductors' topological solutions as well as a generalization of a voltage gain extension cell. However, the dc–ac necessary conversion for grid-connected application as well as the ground issues is not explored in this paper.

This paper presents the first comprehensive review of step-up transformerless single-phase inverter topologies suitable for panel integration. The reviewed topologies are presented in the literature for various specifications; thus, no conclusions can be extracted. Therefore, a typical ac-module application benchmark is set in order to compare the most feasible solutions under the same specifications. Semiconductor and passive components' ratings are selected as a simple method to perform a general comparison in terms of size and cost. These ratings, which are obtained based on simulation results, are affected not only for the set specifications, e.g., European or American grid voltage, but also for the design process, e.g., the selected conduction mode. Considering these constraints, the advantages and disadvantages of the analyzed topologies are discussed in detail as well as their grounding capabilities in order to provide recommendations for the future transformerless module-integrated inverters.

TABLE I
SUMMARY OF THE PV SYSTEMS' INTERCONNECTION STANDARDS [11]–[14]

Issue	IEC 61727		IEEE1547-2008		EN61000-3-2		VDE	
Nominal power	10kW		30kW		16A @ 230V		-	
Harmonic content	order (h)	Limit	order (h)	Limit	order (h)	Limit (A)	order (h)	Limit (A/MVA)
	3-9	4.0%	3-9	4.0%	3	2.3	3	3
	11-15	2.0%	11-15	2.0%	5	1.14	5	1.5
	17-21	1.5%	17-21	1.5%	7	0.77	7	1
	23-33	0.6%	23-33	0.6%	9	0.4	9	0.7
			> 35	0.3%	11	0.33	11	0.5
					13	0.21	13	0.4
	Even harmonics are limited to 25% of the odd harmonic limits shown				(15-39)	2.25/h	17	0.3
							19	0.25
					2	1.08	23	0.2
					4	0.43	25	0.15
					6	0.3	(25-40)	3.75/h
	THD < 5%				(8-40)	1.84/h	even	1.5/h
							>40	4.5/h
DC current injection	Less than 1% of rated output current		Less than 0.5% of rated output current		<0.22A		<1A; max. trip time 0.2s	
Voltage deviations	range (%)	time (s)	range (%)	time (s)	-		range (%)	time (s)
	V<50	0.1	V<50	0.16			V<85	0.2
	50≤V<88	2	50≤V<88	2			V≥110	0.2
	110≤V<120	2	110≤V<120	1				
	V≥120	0.05	V≥120	0.16				
Frequency deviations	range (Hz)	time (s)	range (%)	time (s)	-		range (%)	time (s)
	49<f<51	0.2	59.3<f<60.5	0.16			47.5<f<50.2	0.2
Leakage currents	-		-		-		average current (mA)	time (s)
							30	0.3
							60	0.15
							100	0.04
							300 (peak)	0.3

II. AC-MODULE FEATURES

The microinverter interfaces both the PV module and the grid and it is therefore responsible for two main functions. On the PV side, it must ensure that the maximum available power in the solar panel is extracted, whereas on the grid side, it injects sinusoidal current to the grid. In this section, the PV module and grid requirements are reviewed as well as issues such as the twice line-frequency power decoupling and the grounding technique are discussed.

A. Grid Requirements

As mentioned earlier, the attached microinverter in an ac module is a grid-tie converter, and therefore, it must satisfy the grid connection standards. These standards deal with different issues such as power quality, grid interface and islanding detection, as well as grounding. In Table I, a summary of the main standards regarding the grid connection issues of PV systems is presented [11]–[14].

In terms of power quality, besides the harmonic content of the injected current, a main concern in transformerless topologies is the dc current injection. The standards provide a limit of 1%, or less, of the output rated current, which implies low current values and an increase in the control complexity. Furthermore, the German code VDE0126-1 sets a maximum dc current of 1 A with a maximum disconnection time.

Because of safety reasons for both humans and electronic equipment, the grid-connected inverters must recognize islanding operation [15]. The German code is the most restrictive in the disconnection time due to voltage deviations, while the IEEE standard defines the fastest disconnection time for abnormal frequency operation. The utilized detection methods can be organized into three groups: passive, active, and hybrid methods [15]. Regarding reconnection time, EN50438 [16] standard differentiates between mechanical generators and inverter-based systems. In the last case, the minimum delay for the reconnection is set to 20 s. Furthermore, the German code contemplates the implementation of grid support characteristics such as real power curtailment and reactive power control.

B. Grounding

Based on the survey presented in [8], transformerless topologies are more efficient, lighter, less bulky, and less costly than the isolated inverters. However, when the transformer is left out, the convenient galvanic isolation disappears between the grid and the PV modules. Therefore, leakage ground currents appear due to the solar panel parasitic capacitance between the cells and the grounded frame [9], together with common-mode voltage variations.

Ground currents' evaluation has to be done for each specific topology and the applied modulation technique. In the literature, the influence of the modulation techniques in full-bridge inverters has been analyzed and new topologies have been proposed to minimize the leakage currents [17]–[19]. The proposed topologies can be divided into two main groups: those which introduce decoupling switches in order to avoid the direct connection of the grid and the panels during the current freewheeling, and those which split the solar array in order to connect the neutral to the middle point of the input capacitor and minimize the voltage variations.

In respect to the standards, there is no international agreement in terms of ground current limitations. However, ground currents' monitoring and protections are demanded for most of the previously presented standards. Specifically, the German code VDE 0126-1-1 defines both averaged and peak ground currents' limitations as well as disconnection times (see Table I).

C. PV Module Requirements and Power Decoupling

Nowadays, crystalline silicon PV modules, both monocrystalline and multicrystalline, are the most commonly used within all PV applications. However, thin-film technology has grown in applications where its lower cost compensates a lower efficiency, such as building-integrated PV systems [20]. In Fig. 1, a summary of different solar panel manufacturers is presented for both crystalline silicon (left) and thin-film (right) commercial modules. The data have been extracted from the standard test conditions (STC) measurements available in the modules datasheets. The power generation is lower than 300 W in crystalline silicon modules, with a maximum power point (MPP) voltage range from 25 to 50 V. However, thin-film panels have a higher MPP voltage, from 50 to 100 V, with a lower power generation, up to 150 W.

In single-phase inverters, the instantaneous demanded power consists of a dc value and a twice line-frequency oscillation. As the generated power in the PV module is pure dc, an internal storage device, usually a capacitor, is used in order to maintain the power balance. The value of this decoupling capacitor is determined by the amount of energy to be stored in it. The design of this decoupling capacitor has a significant impact in the utilization ratio of the maximum available power of the PV module [7].

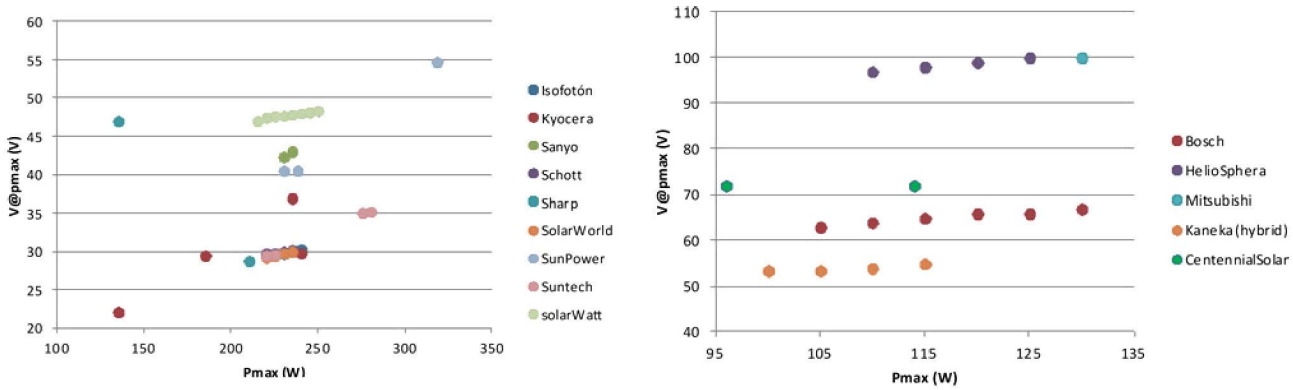

Fig. 1. Maximum power and voltage at MPP (STCs) of crystalline silicon (left) and thin-film (right) commercial modules.

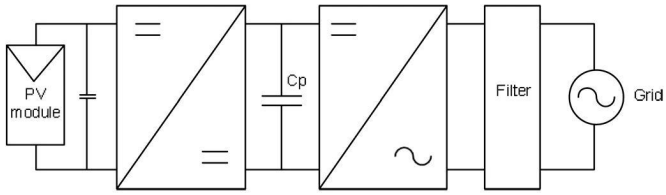

Fig. 2. Block diagram of a two-stage topology for an ac module.

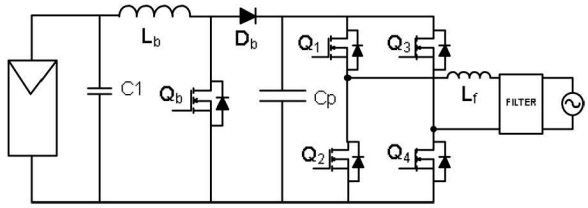

Fig. 3. Boost converter and full-bridge inverter.

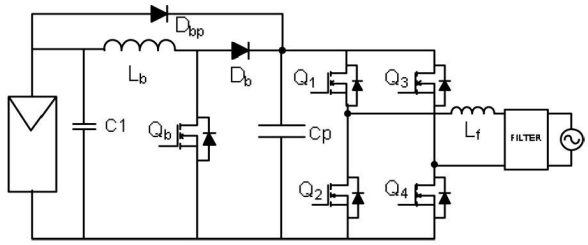

Fig. 4. Time-sharing boost converter with full-bridge inverter [22].

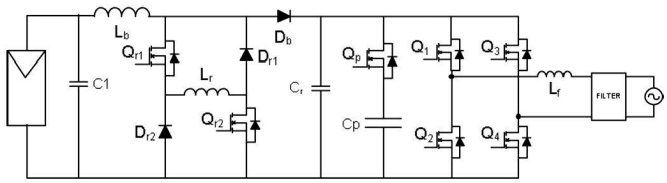

Fig. 5. Parallel resonant soft-switched boost converter and full-bridge inverter [23].

In microinverter applications, the implemented power decoupling technique depends on the specific topology used. Therefore, three decoupling techniques have been identified, depending on the location of the decoupling capacitor and the circuitry: PV-side decoupling, dc-link decoupling, and ac-side decoupling [21]. The utilized technique has a significant influence on the capacitor technology used and, therefore, in the microinverter lifetime. However, the utilization of some of these techniques implies an increase in the circuit complexity and cost as well as additional losses.

III. Step-Up Transformerless Inverters

In this section, a comprehensive review of the existing step-up transformerless single-phase inverter topologies in the literature is presented. The reviewed topologies are classified into three different groups: two-stage, pseudo-dc-link, and single-stage topologies.

A. Two-Stage Topologies

Fig. 2 shows the block diagram of a two-stage topology, also known as topology with dc link. These solutions consist of a dc–dc converter that amplifies the PV module low voltage to an adequate level for the second stage, while performing the MPPT. The dc–ac stage controls the high-performance current injected into the grid by means of pulsewidth modulation (PWM). The power decoupling is done by means of the dc-link capacitor (C_P in Fig. 2). The high voltage level of the dc link allows a lower decoupling capacitance, which improves the life span. Furthermore, since the ripple value of the dc link is not restricted, the capacitance value can be decreased. However, a large ripple may deteriorate the second-stage output current performance.

A conventional configuration consists of the cascade connection of a boost converter and the full-bridge inverter (see Fig. 3). Variations of this configuration [22], [23] have been proposed in order to improve the efficiency of the solution. In [22], a time-sharing dual-mode inverter is proposed (see Fig. 4). In this solution, both the switching and conduction losses of the two stages are reduced by switching one of the stages under sine-wave modulation, while the other does not operate. In [23] (Fig. 5), a soft-switched boost dc–dc converter that achieves both ZVS and ZCS in all the switches is presented. Furthermore, a hysteresis current control that achieves ZVS in the second-stage switches is applied.

In [24], a solution based on a dc–dc converter parallel-input and series-output connected to the solar panel voltage is

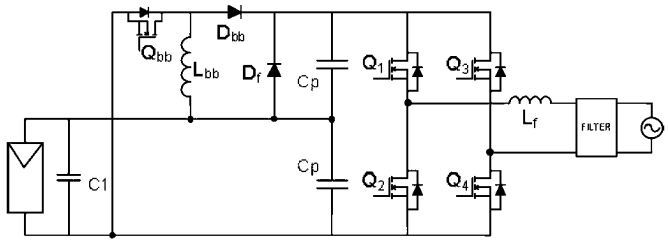

Fig. 6. Parallel-input series-output bipolar dc output converter and full-bridge inverter [24].

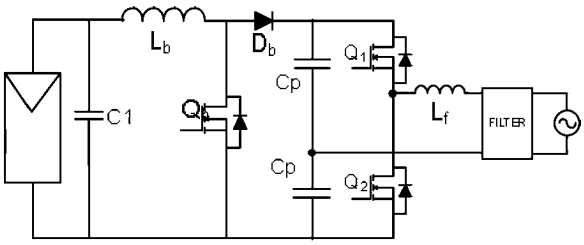

Fig. 7. Boost converter and half-bridge inverter [25].

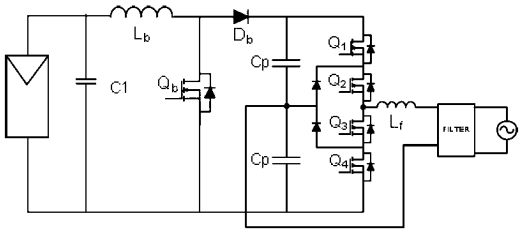

Fig. 8. Boost converter and neutral-point-clamped inverter [26].

presented. This solution seeks to improve the efficiency by means of processing the energy one and half times instead of two times as in the previous presented topologies. Simultaneously, an improvement in the voltage gain of the dc–dc stage is achieved. One of the preferred configurations introduced in [24] is depicted in Fig. 6.

If a half-bridge inverter is used as second stage in the conventional configuration presented in Fig. 3, the number of semiconductors can be reduced (see Fig. 7) [25]. However, the dc-link voltage needs to be twice the grid voltage peak and the semiconductors of the first stage have to block that voltage. Furthermore, the inverter output voltage is bipolar, which increases the filter size. To reduce the filter size, a neutral-point-clamped (NPC) inverter can be used (Fig. 8) [26].

The main advantage of these inverter topologies, half-bridge and NPC, is that the middle point of the dc link is connected to the grid neutral. Therefore, ground leakage currents can drastically be reduced for certain configurations [17].

By using dc–dc converters with bipolar output, as the first stage, the simultaneous grounding of the source and the load can be achieved. Therefore, the ground currents would theoretically be avoided. In [27] and [28], a series combination of boost and buck–boost dc–dc converters is introduced (see Fig. 9). In [29] and [30], some source-grounded bipolar output topologies are reviewed and a topology with coupled inductors is presented, as well as a variation with tapped inductor (see Fig. 10). Both

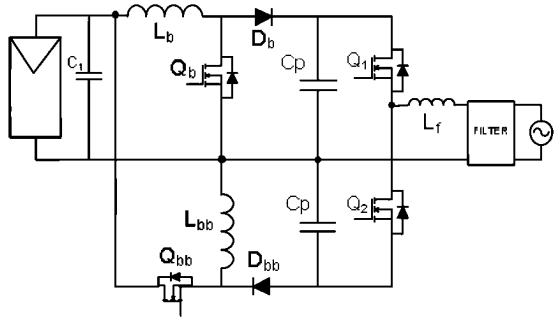

Fig. 9. Series-combined boost and buck–boost and half-bridge inverter [27].

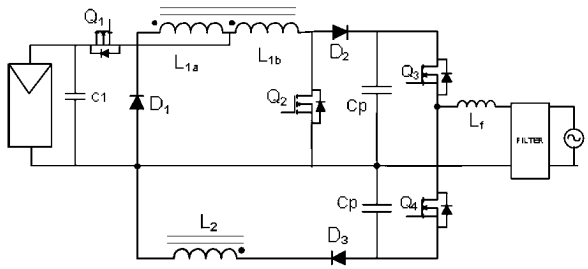

Fig. 10. Center-tapped coupled inductor converter with bipolar output and half-bridge inverter [30].

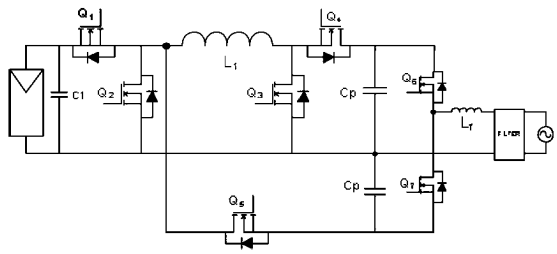

Fig. 11. Single-inductor bipolar output buck–boost converter and half-bridge inverter [31].

topologies have the advantage of a higher boost ratio. Other solutions, such as the one presented in [31], use only one inductor to generate bipolar outputs (see Fig. 11) while maintaining the grounded capability, which is an advantage.

The dual ground capability has also been studied for the classical configuration presented in Fig. 3. As a result, a topology in which some of the switches are shared by the two stages is presented (see Fig. 12) [32]. This topology increases the number of semiconductors and the complexity of the control stage, while high-performance output current (THD lower than 3%) and high efficiency (higher than 94%) are reported.

The main features of the two-stage topology survey are presented in Table II. The results for topologies shown from Figs. 8–11 and 6 are not included since results for one of the stages are only seen, or there is no available information.

B. Pseudo-DC-Link Topologies (DC/DC and Unfolding Converter)

The topologies included in this category are based on a dc–dc converter that generates a rectified sinusoidal current, and implements the MPPT functionality. This current is then unfolded

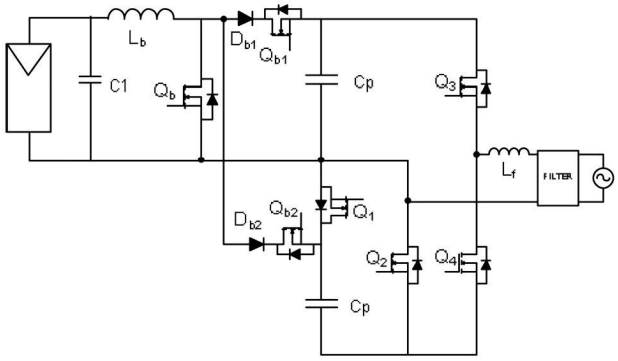

Fig. 12. Boost + FB integrated and dual grounded [32].

TABLE II
SUMMARY OF THE DISCUSSED TWO-STAGE TOPOLOGIES

Figure	Vin (V)	Po (W)	Vo (Vrms)	fs (kHz)	max eff(%)
Fig. 3	160	1500	200	20	94
Fig. 4	160	1500	200	20	96.5
Fig. 5	100	250*	120	30	-
Fig. 7	120	850	230	6.26	-
Fig. 12	175	931	120	18	96.7

*Estimated.

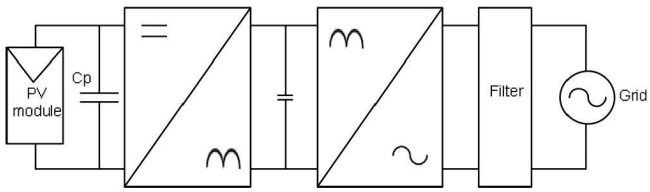

Fig. 13. Block diagram of a pseudo-dc-link topology for an ac module.

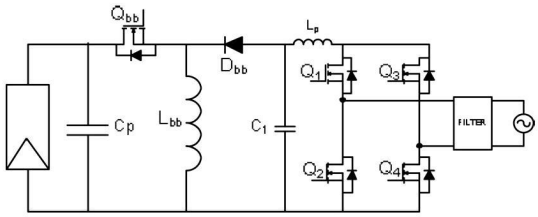

Fig. 14. Buck–boost DCM converter and unfolding stage [33].

in phase with the grid by means of a line-switched bridge. As in the previous topologies, the power decoupling is usually done by a capacitor. However, in this case, the capacitor is in parallel with the PV module (C_P in Fig. 13). Therefore, the allowable voltage ripple must be low enough to ensure a high MPPT efficiency. This fact together with the low voltage level implies that a large capacitance is necessary [21]. In most of the cases, an electrolytic capacitor is used, which may reduce the life span of the solutions.

The buck–boost converter operated in discontinuous conduction mode (DCM) behaves as a current source. Using this characteristic, both inverting (see Fig. 14) [33] and noninverting (see Fig. 15) [34] buck–boost converters have been utilized as grid interfaces in PV systems, following the scheme presented in Fig. 13.

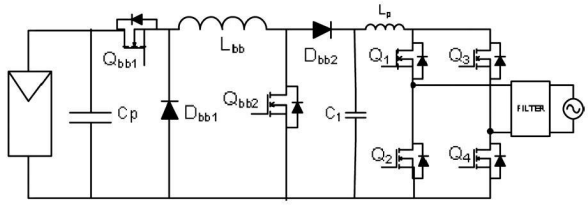

Fig. 15. Noninverting buck–boost DCM converter and unfolding stage [34].

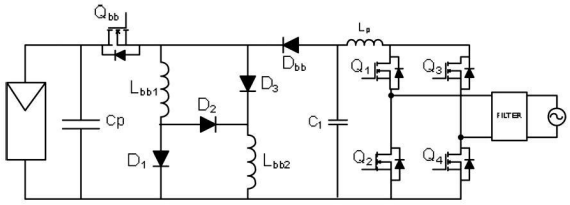

Fig. 16. Switched-inductor buck–boost DCM converter and unfolding stage [35].

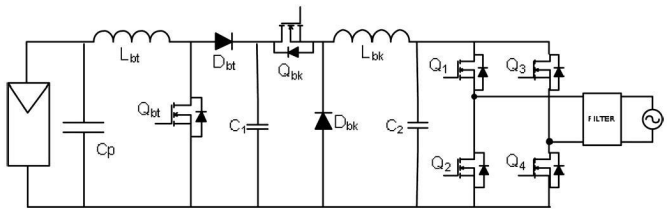

Fig. 17. Boost–buck time-sharing converter and unfolding stage [36].

TABLE III
SUMMARY OF THE DISCUSSED PSEUDO-DC-LINK TOPOLOGIES

Figure	Vin (V)	Po (W)	Vo (Vrms)	fs (kHz)	max eff(%)
Fig. 14	50	150	100	10	-
Fig. 15	16*8	200	110	10	70
Fig. 16	20	170	230	10	85
Fig. 17	200-400	1000	230	-	98.5

Using the same operation mode, a switched-inductor buck–boost inverter is introduced in [35]. This inverter, depicted in Fig. 16, achieves an increase of $\sqrt{2}$ in the gain of the converter compared to the classical DCM buck–boost converter, while the efficiency remains practically the same.

In the previous solutions, the efficiency is expected to be low due to the operation mode, e.g., 85% @ 170 W has been reported in [35]. In [36] and [37], a high-efficiency PV inverter for 1-kW application is introduced (see Fig. 17). This inverter is based on the cascaded connection of a boost and a buck converter to generate the rectified sinusoidal current. The reported high efficiency (approximately 98% @ 1 kW) is achieved applying the time-sharing concept introduced in [22], i.e., the converter operates either as buck or boost mode depending on the instantaneous grid voltage. The topology survey main features for the pseudo-dc-link topologies shown in this section are presented in Table III.

C. Single-Stage Topologies

In the last years, the tendency is to reduce the number of power stages in order to increase the overall efficiency and the

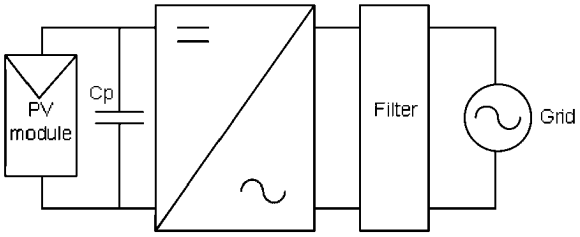

Fig. 18. Block diagram of a single-stage topology for an ac module.

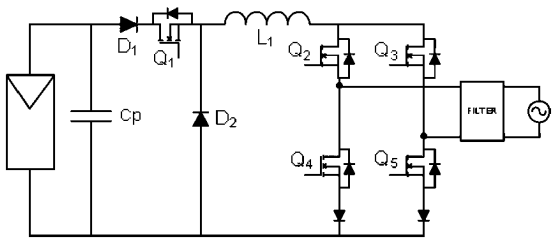

Fig. 19. Universal single-stage grid-connected inverter [38].

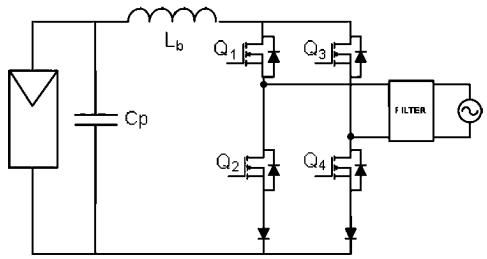

Fig. 20. Integrated boost inverter [40].

reliability of the proposed solutions, as well as reduce the cost of the increasing power density. The pseudo-dc-link topologies presented in the previous section constitute a step toward this trend. Nowadays, the trend is the integration into a single-stage converter (see Fig. 18), which includes all the desired functionalities developed by the multistage topologies. As in the pseudo-dc-link topologies, the power decoupling in single-stage topologies is done by means of a capacitor in parallel with the PV module (C_P in Fig. 18).

Several topologies have been proposed based on either boost or buck–boost principles. A single-stage topology that can operate as a buck, boost, or buck–boost is presented in [38] (Fig. 19). This solution can operate with a wide range of input voltage, improving the efficiency, since it is able to work at the most appropriate configuration for each operating condition. In [39], the same topology with a hysteresis control strategy is analyzed for standalone applications, achieving low-voltage total harmonic distortion (THD).

In [40], the resulting integration of the boost converter and the full-bridge, shown in Fig. 20, is presented.

As a boost converter cannot generate output voltages lower than the input voltage, a zero cross current distortion is expected. The boost dc–ac converter introduced in [41] (see Fig. 21) solves this problem by connecting to the grid two dc–dc boost converters differentially. Each of the converters generates a dc-biased unipolar sinusoidal voltage 180° out of phase one to the other.

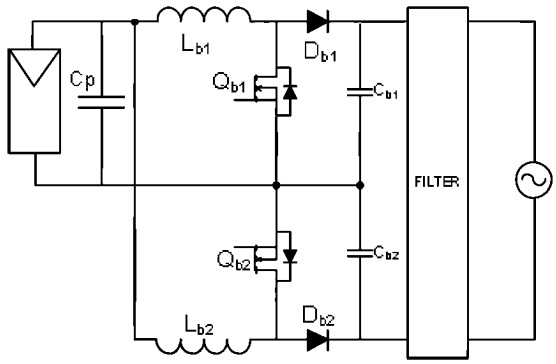

Fig. 21. Differential boost inverter [41].

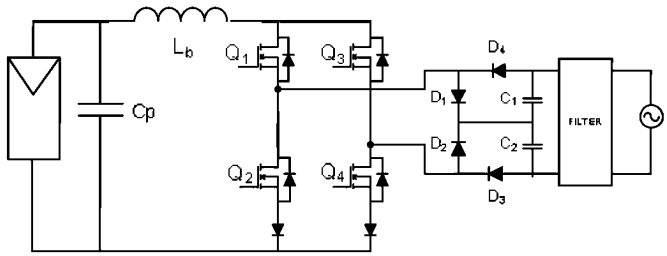

Fig. 22. Boost inverter with improved zero crossing [42].

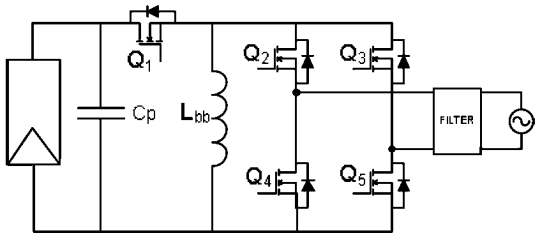

Fig. 23. Integrated buck–boost inverter [40].

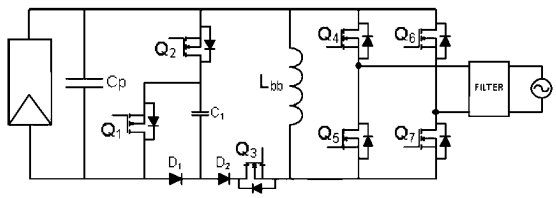

Fig. 24. Buck–boost inverter with extended input voltage range [44].

The same principle is used in the boost inverter presented in [42] (see Fig. 22). In the integrated solution mentioned earlier (see Fig. 20), the use of the tri-state modulation [43] is analyzed in order to improve the current zero crossing. The application of this modulation requires an additional switch to achieve the inductor current freewheeling state.

As mentioned previously, the integration of the boost converter and the full-bridge converter is presented in [40]. The utilization of any other dc–dc converter is suggested, and the integration of the buck–boost converter (see Fig. 23) with the full-bridge inverter is introduced. A variation of this topology (see Fig. 24) that allows a wider input voltage range is presented in [44].

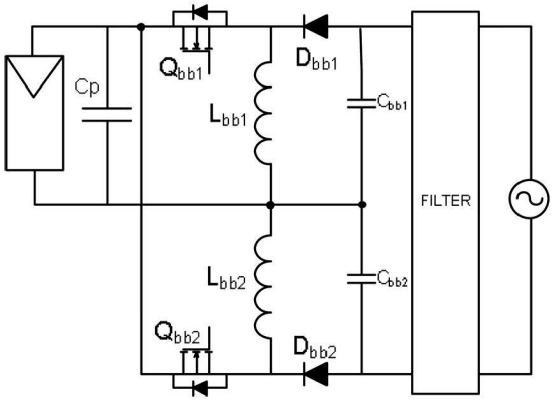

Fig. 25. Differential buck–boost inverter [45].

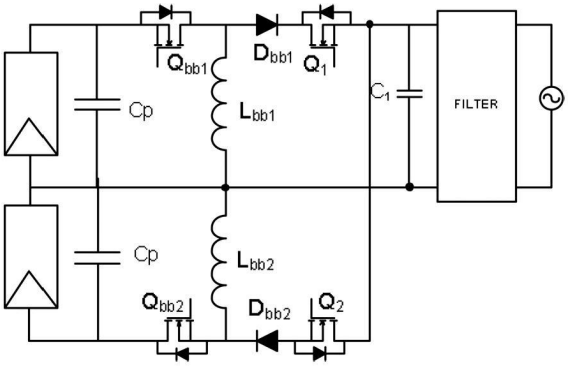

Fig. 26. Two-sourced antiparallel buck–boost inverter [46].

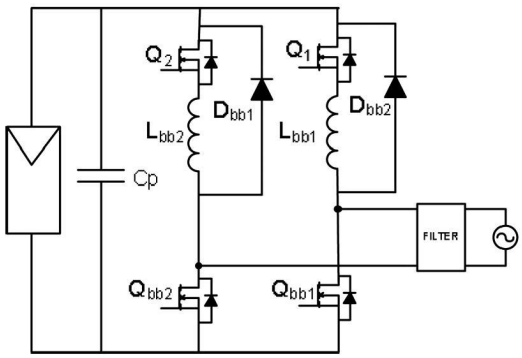

Fig. 27. Single-stage full-bridge buck–boost inverter [47].

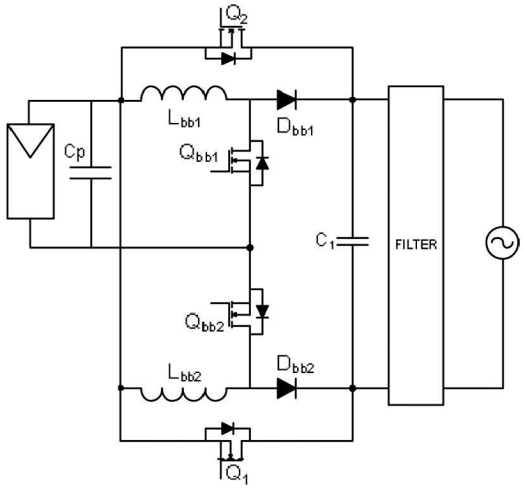

Fig. 28. Buck–boost-based single-stage inverter [48].

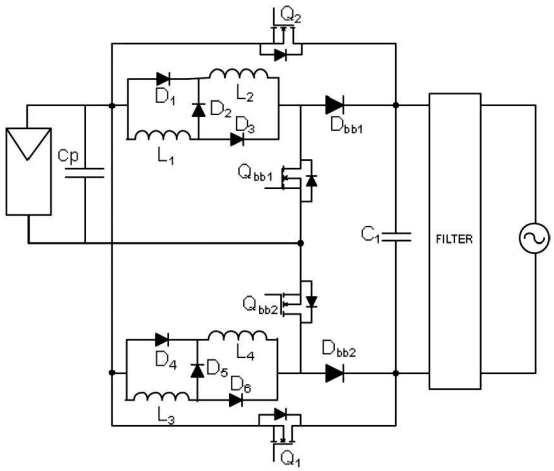

Fig. 29. Switched-inductor buck–boost-based single-stage inverter [49].

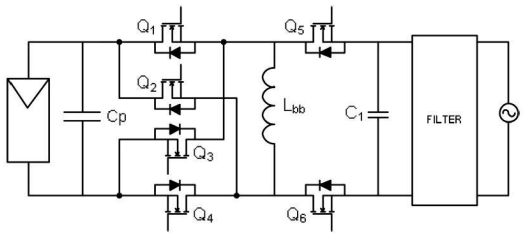

Fig. 30. Single-inductor buck–boost-based inverter [51].

As well as for the boost topology seen in Fig. 21, the dc-biased sinusoidal differential configuration has been studied for the buck–boost converter (see Fig. 25) [45]. However, other configurations using two converters working alternatively for each positive and negative grid voltages have been proposed. In the inverter presented in [46] (see Fig. 26), two buck–boost converters with their own solar panel, or two different sections of the same panel, are connected in antiparallel. Each converter operates in DCM at the corresponding part of the grid cycle.

The same principle and operation mode is applied to the topologies introduced in [47] and [48]. However, these two inverters, as depicted in Figs. 27 and 28, respectively, are using a common source. The configuration presented in Fig. 28 is preserved in [49], but the inductor is substituted by a switched-inductor network (see Fig. 29). This substitution achieves an $\sqrt{2}$ increase in the voltage gain. A higher increase in the voltage gain is obtained in the center-tapped topology introduced in [50], keeping the configuration shown in Fig. 28.

The topologies shown from Figs. 25–29 are based on two relatively independent converters that operate for each half-cycle. However, some topologies, such as proposed in [51] (see Fig. 30), [52] (see Fig. 31), and [53] (see Fig. 32), share the passive components, thus increasing the compactness, the number of switches, as well as the complexity in the control.

Some of the existing solutions share the passive components to reduce the semiconductor number by means of coupled

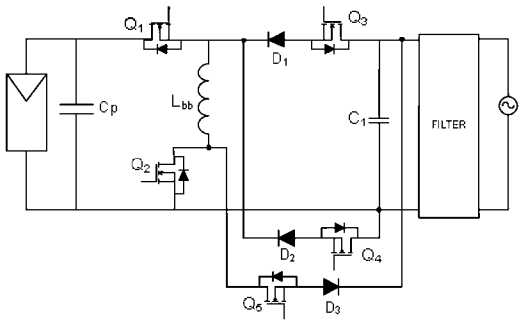

Fig. 31. Doubly grounded single-inductor buck–boost-based inverter [52].

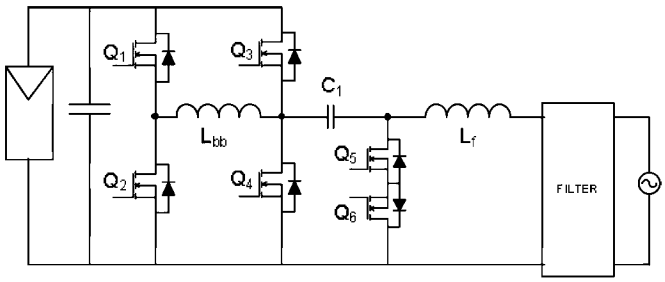

Fig. 32. Single-inductor buck–boost-based inverter with dual ground [53].

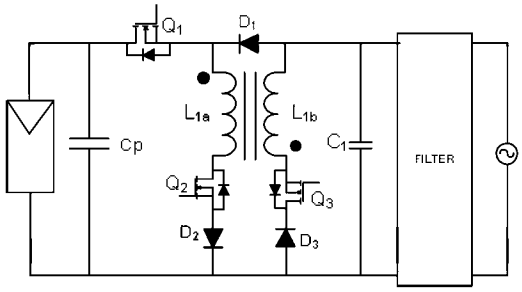

Fig. 33. Three-switch buck–boost inverter [54].

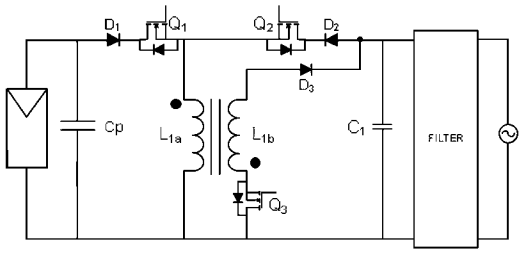

Fig. 34. Coupled inductor buck–boost inverter [55].

inductors. This is the case of the topologies presented in [54] (see Fig. 33) and [55], [56] (see Fig. 34), where the coupled inductors work as an inductor during the negative half-cycle and as a flyback transformer for the positive one.

All the solutions presented in this section are based on boost or buck–boost principle. However, in [57], an inverter based on the impedance–admittance conversion theory is introduced. The converter, depicted in Fig. 35, transforms a high-frequency voltage into a high-frequency current by means of an immittance conversion circuit (four terminal *LC* network). Afterward, a cycloconverter generates the line-frequency current that is injected

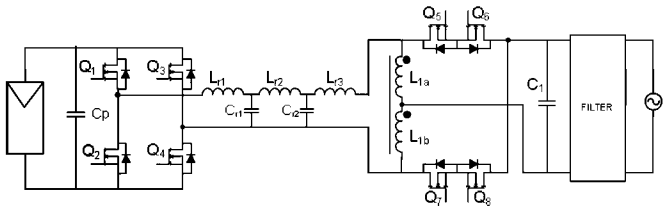

Fig. 35. Impedance–admittance conversion theory-based inverter [57].

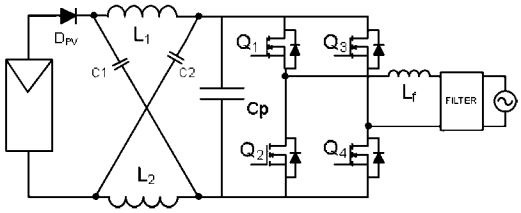

Fig. 36. Single phase Z-source inverter.

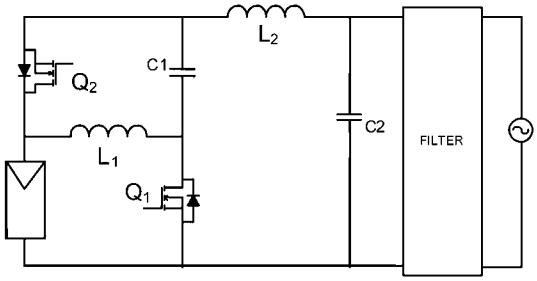

Fig. 37. Semi quasi-Z-source inverter with continuous voltage gain [60].

into the grid. Despite the high number of passive components, the compactness of the solution is still high, since the *LC* network resonant frequency is much higher than the grid frequency.

Other energy conversion technique, mostly used in three-phase applications, is the Z-source inverter [58]. This family of converters can provide boosting capabilities to conventional H-bridge inverters by adding an *LC* impedance network in the front end of the converter (see Fig. 36). In recent years, single-phase topologies have been presented for Z-source or modified Z-source inverters. The dual ground capability, desirable in PV applications, has also been studied and topologies with lower switch counting were presented (see Fig. 37) [59], [60]. The main drawback of these inverters is the limited practical conversion range, which limits the use of these inverters suitable for ac-module application. As an attempt to improve the voltage gain, in [61], switched-inductor and switched-capacitor structures are analyzed and generalized. As a result, an improvement in a factor of above 2 can be achieved using one switched-inductor cell.

Table IV summarizes the performance of the single-stage topologies discussed in this section.

IV. Comparison of Topologies Under AC-Module Operating Conditions

Tables II–IV of the previous section summarize the main features of the reviewed topologies. No conclusions can be drawn

TABLE IV
SUMMARY OF THE DISCUSSED SINGLE-STAGE TOPOLOGIES

Figure	Vin (V)	Po (W)	Vo (Vrms)	fs (kHz)	max. eff.(%)
Fig. 19	100-200	500	230	10	-
Fig. 20	25	200	127	-	-
Fig. 21	100	500	127	30 (max)^	-
Fig. 22	60	400*	110	-	-
Fig. 24	100	640	100	17 (max)^	-
Fig. 25	50	200	120	-	
Fig. 26	48	500	100	9.6	80
Fig. 27	75	500	110	10	-
Fig. 28	90	300	110		87
Fig. 29	20	60*	230	10	-
Fig. 30	30	50	110	70	87 (50% load)
Fig. 31	92	170	100	10	87*
Fig. 33	50	1000	70	10	-
Fig. 34	50-300	1000	120	5	-
Fig. 37	160	200	110	20	94,5

^Variable frequency operation.
*Estimated.

from these summaries since the topologies are designed for different power, voltage, and frequency specifications. Therefore, in order to compare the reviewed topologies properly, a typical benchmark is set in this paper.

A. Benchmark Settings

The following design specifications have been considered for the detailed comparison, based on the features analyzed in the first section.

1) The output voltage and power of the solar panel have been set to 30 and 250 W, respectively. These values correspond to a standard crystalline PV module, as shown in Fig. 1.
2) The microinverter is connected to U.S. grid (120 V @ 60 Hz). U.S. grid is selected since the necessary voltage gain is half as a comparison to the EU grid and, therefore, more adequate for transformerless topologies. However, as a result of the comparison, it will be shown that new topologies with high gain capability are required.
3) The used switching frequency is 40 kHz for dc–ac stage, in the two-stage topologies, and for all the pseudo-dc-link and single-stage topologies.
4) In dc–dc stages of two-stage topologies, a switching frequency of 80 kHz is used.
5) A maximum ripple of 5% has been set for both the dc-link voltage and the input voltage, to ensure the extraction of the maximum available power.
6) DC-link voltage in the two-stage topologies is 200 V, except the topologies with half-bridge as a second stage in which the bus voltage is 360 V.
7) The maximum allowable current ripple is 20% for the converters operating in continuous conduction mode (CCM). In case the converter operates in DCM, the inductance has been selected to ensure DCM for the whole operating range.

TABLE V
SIMULATION RESULTS AND DESIGN PARAMETERS UNDER THE BENCHMARK SETTINGS

Topology	Solution	Dual Grounding	Dmax (USgrid)	Components rating			Mode
				Inductors (mJ)	Dec. Cap. (J)	Semiconductors (kVA)	
Fig. 3	A.1	NO	0.85	13,98	3,32	15,10	CCM
Fig. 7	A.2	NO	0.92	14,61	3,37	11,96	CCM
Fig. 9	A.3	YES	0.87	14,58	4,00	13,41	CCM
Fig. 14	B.1	NO	0.68	18,00	3,33	22,72	DCM
Fig. 15	B.2	NO	0.68	18,00	3,33	22,65	DCM
Fig. 17	B.3	NO	0.85	41,00	3,33	12,65	CCM
Fig. 20	C.1	NO	0.81	31,00	3,33	31,65	CCM
Fig. 21	C.2	NO	0.85	32,00	0,09	10,42	CCM
Fig. 25	C.3	NO	0.76	16,00	0,09	16,71	DCM
Fig. 26**	C.4	YES	0.68	25,00	12,60	30,75	DCM
Fig. 28	C.5	NO	0.68	26,00	3,33	33,39	DCM
Fig. 30	C.6	NO	0.68	13,00	3,33	48,41	DCM
Fig. 31	C.7	YES	0.68	13,00	3,33	43,05	DCM

**: two modules or two sections of 30V/125W.

B. Comparison Criteria and Results

The 13 most feasible solutions presented in the previous section have been designed and simulated according to the set benchmark. The selected topologies are considered to be representative of their group and the obtained results can be extrapolated to the rest of solutions. Passive and semiconductor ratings, obtained based on simulation results, are used as a simple method to compare the selected topologies in terms of size and cost [7]. The passive component rating consists of the stored energy in the decoupling capacitor and the inductors (1). The considered semiconductor rating is based on the product of the peak voltage and the RMS current withstood by the semiconductor (2). In (1) and (2), n_I and n_{Sc} are the number of inductors and semiconductors, respectively. The inductance values resulting of the design process are shown in Appendix A

$$\mathrm{PR} = \sum_{k=1}^{n_I} \frac{1}{2} \cdot L_k \cdot {I_{L_{k\_\mathrm{pk}}}}^2 + \frac{1}{2} \cdot C_p \cdot {V_{c_p\_\mathrm{pk}}}^2 \tag{1}$$

$$\mathrm{ScR} = \sum_{i=1}^{n_{\mathrm{Sc}}} V_{\mathrm{max}_i} \cdot I_{\mathrm{RMS}_i}. \tag{2}$$

These ratings together with the dual ground capability, the mode of operation, and the maximum ideal duty cycle applicable in the analyzed topologies, presented in Table V, compose the criteria used for the selected topologies comparison.

The introduced parameters are not only influenced by the set specifications but also by the design process. Maximum applicable duty cycle is a clear example of benchmark-affected parameter. Furthermore, passive component ratings are also affected for the set specifications since the set switching frequency for dc–dc stages is twice the frequency for dc–ac stages. With respect to the design process, the selected mode of operation affects the semiconductors rating, e.g., buck-based topologies are designed in DCM, thus increasing the RMS currents but simplifying the control stage. These constraints have been taken into account in the discussion of the next section.

In the case of dual grounding capability, three of the analyzed topologies present this capability, thus avoiding ground currents. However, the other solutions can be modified to reduce or even eliminate the leakage currents as it will be discussed in the next section. These modified topologies have not been included in

TABLE VI
GENERAL ISSUES OF THE ANALYZED TOPOLOGIES UNDER THE BENCHMARK SETTINGS

Topology	Solution	Power decoupling	Number of				Grid interface	Filter
			Inductors*	Cap:F(E)^	Transistors	Diodes		
Fig. 3	A.1	166uF@200V	2	2{0}	5	1	VSI 4T	LCL
Fig. 7	A.2	52uF@360V	2	3{0}	3	1	VSI 4T	LCL
Fig. 9	A.3	2x100uF@200V	2	3{0}	4	2	VSI 2T	LCL
Fig. 14	B.1	7,4mF@30V	2	1{1}	5	1	CSI 4T	CL
Fig. 15	B.2	7,4mF@30V	2	1{1}	6	2	CSI 4T	CL
Fig. 17	B.3	7,4mF@30V	2	2{1}	6	2	CSI 4T	CL
Fig. 20	C.1	7,4mF@30V	1	0{1}	4	2	CSI 4T	CL
Fig. 21	C.2	2x100uF@30V	2	3{0}	2	2	CSI 2T	CL
Fig. 25	C.3	2x100uF@30V	2	3{0}	2	2	CSI 2D	CL
Fig. 26**	C.4	2x14mF@30V	2	1{2}	4	2	CSI 2T	CL
Fig. 28	C.5	7,4mF@30V	2	1{1}	4	2	CSI 2T	CL
Fig. 30	C.6	7,4mF@30V	1	1{1}	6	0	CSI 2T	CL
Fig. 31	C.7	7,4mF@30V	1	1{1}	5	3	CSI 3T	CL

**: two modules or two sections of 30V/125W
^: Film (F) and Electrolitic (E) capacitors
*: inductor of the CL component of the output filter not considered

the analysis since the required detailed comparison is out of the scope of this paper.

In addition to the presented criteria, Table VI shows other general issues derived from the design process that will be discussed in the next section:

1) the grid interface together with the required type of filter;
2) the necessary capacitance for a correct power decoupling; and
3) the number of passive components and semiconductor devices.

As an example of the developed simulations, Fig. 38 shows the inductor currents as well as the drain to source and output voltages of the series-connected boost (upper part) and buck–boost (bottom part) converters that compose the first stage of the solution presented in Fig. 9.

Fig. 39 shows the simulated inductor currents for the single-stage topology presented in Fig. 26. As can be seen, each converter is operating in DCM during the proper half part of the grid voltage.

C. Discussion

In this section, a discussion for both the general issues and the design and simulation obtained ratings is presented.

1) General Issues: An essential issue in grid-connected inverters is the output filter. As shown in Table VI, two different grid interfaces can be considered and, therefore, two kinds of output filter. In the two-stage topologies, the interface is a voltage source inverter (VSI) that generates a sinusoidal current to be injected into the grid by applying the dc voltage, with the proper polarity, and zero voltage. An *LCL* filter is used in these cases. The inverter-side inductor of the *LCL* filter (L_f in Fig. 3) plays an essential role in the behavior of the VSI inverter, since it enables the necessary output current control in grid-connected applications. The *CL* filter component is designed to improve the grid current quality to comply with the quality standards. However, pseudo-dc-link or single-stage configurations are current source inverters (CSIs) in which the converter is controlled to follow either a rectified or a pure sinusoidal current. Then, the current is injected into the grid by unfolding the rectified sinusoidal current such as in pseudo-dc-link configurations or by the proper control of single-stage configurations. Therefore, in order to present a fairer comparison, the *CL* components of the output filter for both CSI and VSI have not been considered.

In terms of power decoupling, pseudo-dc-link and single-stage topologies use a bulky electrolytic capacitor in parallel with the PV module, thus limiting the lifetime of the microinverter [21]. In the case of two-stage topologies, a lower capacitance in the dc link can be used allowing utilization of different capacitor technology and increasing the life span of the integrated inverters. Accordingly, some of the analyzed single-stage configurations such as the ones based in the differential connection of two boost (C.2) or buck–boost (C.3) converters reduce drastically the parallel capacitor. Therefore, the possibility of using longer lifetime capacitor technologies can be explored for these configurations. Furthermore, these solutions allow a capacitor size reduction with respect to other solutions. On the other hand, solution C4 needs more capacitance for a proper power decoupling, thus increasing the capacitor size.

2) Design- and Simulation-Based Parameters' Comparison: As set in the benchmark, the U.S. grid voltage and frequency are considered in the comparison with a dc-link voltage of 200 V. As an exception, the dc-link voltage has been increased to 360 V for the topology of Fig. 7, which uses a half-bridge inverter as second stage. In these cases, the maximum obtained ideal duty cycle in the solutions operating at CCM is higher than 0.85, which implies difficulties in the converter implementation. This situation is even worse in the case of connection to the European grid as the voltage is doubled. Several high step-up converters have been proposed in the literature [10] as an alternative to the boost converter. Furthermore, the combination of these high step-up dc–dc converters together with the reviewed step-up inverter topologies could help with the necessary voltage gain to achieve both U.S. and EU grid.

Based on simulation results, both semiconductor and passive component ratings have been calculated. In the previous section, capacitor technology and size have been analyzed. Most of the analyzed solutions present similar capacitor component rating. Therefore, the size is analyzed based on the calculated inductor rating. Fig. 40 shows a comparison of the results introduced in Table V in respect to the inductor and semiconductor calculated ratings.

As a result of the obtained results, two-stage configurations are the best positioned in both ratings. It should be emphasized here that the switching frequency set for the dc–dc converters were doubled compared to the stages that withstand with the ac component. These topologies present easy control stages since MPPT and current injection are decoupled in the different stages. However, ground leakage currents appear if a full-bridge inverter is used as a second stage. Ground currents in full-bridge derived inverters are well known and have been deeply studied; thus, several solutions that allow to comply with the regulations have been proposed [8], [17]–[19], [32], [62]–[64]. These solutions might also be used in this application. However, the topologies are based on either dc or ac decoupling

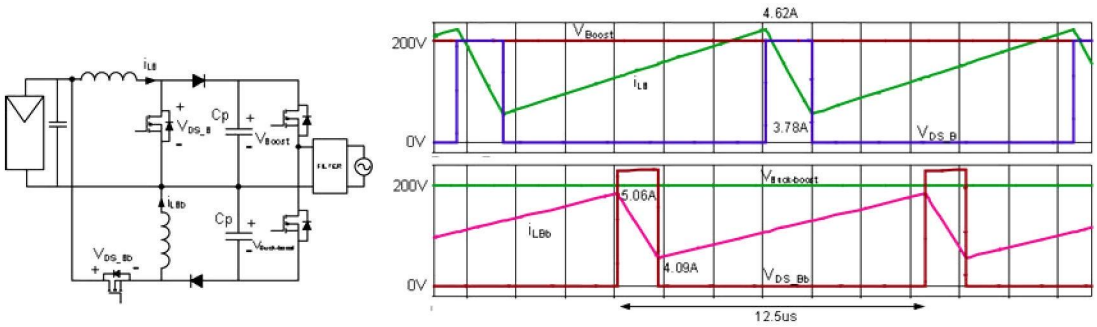

Fig. 38. Simulated waveforms of the dc–dc converter in the two-stage topology presented in Fig. 9.

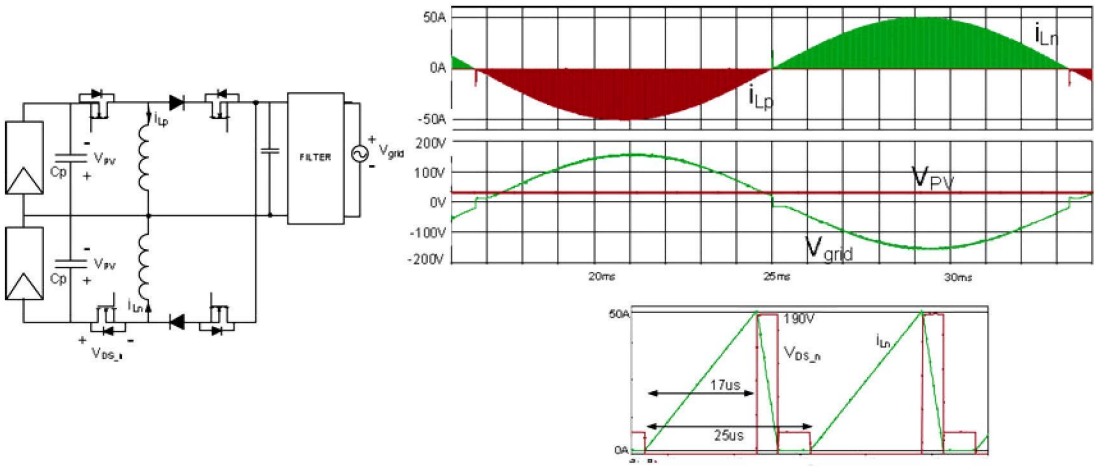

Fig. 39. Simulated waveforms in a grid period and detail of maximum duty cycle of the single-stage topology presented in Fig. 26.

switches [17], and therefore, more devices are necessary. An appropriate alternative is the use of a half-bridge inverter as second stage since the device counting is reduced and ground currents can be drastically reduced or eliminated. Therefore, the analyzed solution A.3 that allows dual grounding is the preferred configuration.

Detailed simulations of this solution together with solutions B.1 and C.7 have been performed using the semiconductor and inductor models shown in Appendix B. These three topologies present low or no leakage current and can be considered as a representative of each topological group shown in Table VI.

In analyzed solutions A.1 and A.2, the number of high-frequency switched semiconductors and inductors is half than in topology A.3. Therefore, their efficiency is expected to be slightly higher than the efficiency of A.3 presented in Fig. 41.

Analyzed pseudo-dc-link topologies have similar cost and size than two-stage solutions. Furthermore, efficiency variation with the output power is flatter than for the two- or single-stage analyzed topologies (see Fig. 41), thus achieving the highest weighted efficiency (93%). Despite the solution B.3 could achieve an improvement in the efficiency of the solution B.1 due to the applied time-sharing strategy, its size is clearly higher due to the necessary big inductors to ensure CCM. In terms of ground currents, as the interface bridge is a low-frequency

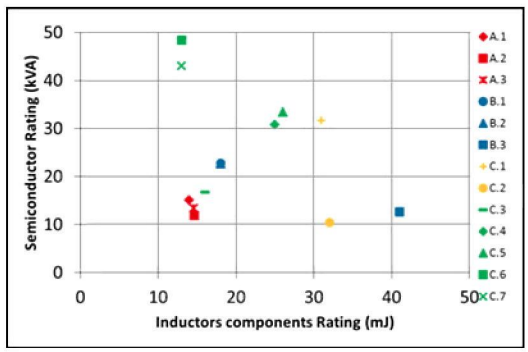

Fig. 40. Semiconductor and inductor component ratings for the simulated configurations; red: two-stage (A solutions in Table VI), blue: pseudo-dc-link (B solutions in Table VI), yellow: single-stage boost based, green: single-stage buck–boost based (C solutions in Table VI).

unfolding stage, ground leakage currents are low. In [65], the decoupling of the solar panel and the grid during freewheeling time is applied in solutions B.1 and B.2, like in full-bridge derived topologies. Therefore, leakage ground currents can be eliminated. However, more switches are necessary and the inductor has to be split since a symmetrical configuration of the converter in the dc side is necessary.

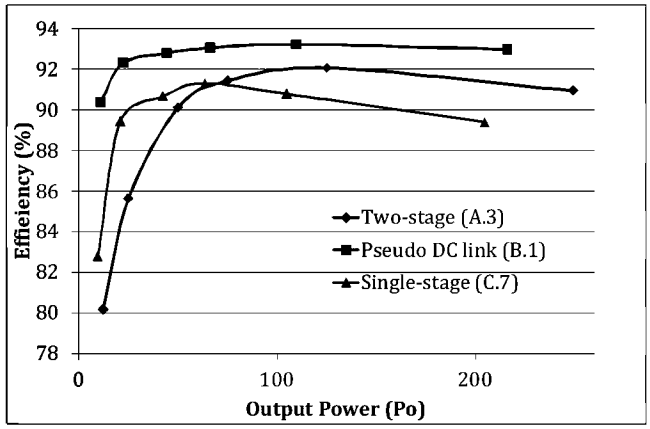

Fig. 41. Estimated efficiency of representative topologies A.3, B.1, and C.7 of each presented group.

The analyzed boost-based single-stage inverters (solutions C.1 and C.2) present higher size than the previous topologies, except solution B.3. Solution C.1 is more expensive and the expected current THD is high due to the zero-crossing distortion. Solution C.2 corrects this drawback by means of the differential connection while using less semiconductor devices. Furthermore, the negative dc side is connected to the middle point of the output capacitors. Therefore, the negative dc-side voltage is more stabilized and the ground currents will be reduced, as in half-bridge inverters [32]. The same differential configuration is used in solution C.3 for buck–boost converters. Based on the obtained ratings, this solution is smaller than the previous one with a similar cost, presenting equivalent ratings to the two-stage analyzed inverters. However, the RMS currents in the buck–boost-based solution (C.3) are twice than in the boost-based one (C.2), and the inductor current peak is four times bigger, according to the simulation results. This increase is due to the discontinuous operation mode; thus, the expected efficiency is lower than that obtained for topology C.7 (see Fig. 41).

The rest of the buck–boost-based single-stage analyzed topologies (solutions C4–C7) have a higher cost than the analyzed two-stage topologies. Due to the operation in DCM, the RMS currents and, therefore, the obtained semiconductor ratings are high. According to the simulation results, RMS currents and inductor peak current are at least 43% bigger and five times higher, respectively, in the DCM buck–boost operated topologies than in the CCM boost converter of solution A.1. Despite only one transistor (or two in the case of C.7) is high frequency switched in the analyzed topologies, the efficiency is not expected to be high due to the aforementioned RMS currents, as the simulation presented in Fig. 41 confirms with a weighted efficiency of 90.2%.

Furthermore, since these topologies (from Figs. 26–34) are based on two more or less independent converters, an important concern is the dc current injection. The behavior of the most of the reviewed topologies is symmetric. However, in the case of the analyzed topology C.7 (see Fig. 31), transistor Q2 is switched either constantly ON for negative grid voltage or under PWM modulation when the grid voltage is positive, thus complicating the control stage.

In respect to leakage currents, the simulated solutions C.4 and C.7, as well as the topologies depicted in Figs. 32–34, allow dual grounding of the grid and the dc side, thus theoretically eliminating ground currents. In solutions C.5 and C.6, either the positive (C.5) or the negative (C.6) dc side is connected to both the grid neutral or the grid line, depending on the grid half-cycle, through low-frequency switches. Therefore, the dc-side voltages have a big low-frequency component and the ground leakage currents are expected to be low. Furthermore, the dc-side transistors in C.6 (see Fig. 30) would allow a dc-side decoupling like in full-bridge inverters by means of complicating the control strategy and, therefore, increasing the losses since more transistors would be high-frequency switched.

V. Conclusion

In this paper, a comprehensive review of single-phase nonisolated inverters for ac-module applications is presented. Both the grid connection and the solar panel requirements are analyzed emphasizing the leakage current regulation, as it is a main concern in nonisolated PV grid-connected inverters. In order to compare the most suitable solutions of the reviewed topologies under the same specifications, a benchmark of a typical ac-module application is set. These solutions have been designed and simulated, obtaining ratings for the passive and the semiconductor components. These ratings are used for the topology comparison in terms of size and cost. Furthermore, detailed simulations of representative topologies have been performed using semiconductor and inductor models to estimate the efficiency of the reviewed solutions. As a result of the comparison, the required voltage boost necessary for the connection to the European grid is difficult to achieve with transformerless topologies, but it is adequate for U.S. requirements. Two-stage topologies, including the solution with dual grounding capability that theoretically avoids the ground leakage currents, are the preferred option for the set benchmark in which switching frequency for the dc–dc stage is set twice than for the dc–ac one. The two-stage combination of a step-up dc–dc converter and a step-up inverter should be considered. In addition, the analyzed pseudo-dc-link approaches are an alternative solution in terms of size and cost. Furthermore, ground currents are expected to be low in these solutions because of the line-frequency interface and weighted efficiency is the highest due to the flat behavior of the efficiency with the output power. The analyzed single-stage topologies have higher cost than the other analyzed solutions and control is expected to be more complex to avoid dc current injection. In addition, DCM operation mode allows smaller solutions, including a solution with dual ground capability, but efficiency is lower due to the high RMS currents.

Appendix A

This appendix shows the inductance value utilized for the simulations presented in Section IV-B. The designed inductances comply with the benchmark set in Section IV-A.

Topology	Inductance value	
Fig. 3	L_b=191µH	L_f=1,15mH
Fig. 7	L_b=206µH	
Fig. 9	L_b=382µH	
	L_{bb}=332µH	
Fig. 14	L_{bb}=10µH	Lf=1mH
Fig. 15		
Fig. 17	L_{bt}=191µH	L_{bk}=1,34mH
Fig. 20	L_b=182µH	
Fig. 21	L_{b1}=382µH	L_{b2}=382µH
Fig. 25	L_{bb1}=20µH	L_{bb2}=20µH
Fig. 26	L_{bb1}=10µH	L_{bb2}=10µH
Fig. 28		
Fig. 30	L_{bb}=10µH	
Fig. 31		

APPENDIX B

The simulation models used for the detailed simulations are MBR40250G (diode), IRFB4332PBF (MOSFET), and IRFP4668PBF (unfolding stage). The inductors have been designed with PExprt using RM cores. PSPICE models for the inductor have been obtained using the finite-element tool PEmag.

REFERENCES

[1] "Global Market Outlook for Photovoltaics until 2015," *European Photovoltaic Industry Association,* 2011.

[2] B. Liu, S. Duan, and T. Cai, "Photovoltaic DC-building-module-based BIPV system—Concept and design considerations," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1428–1429, May 2011.

[3] N. Femia, G. Lisi, G. Petrone, G. Spagnuolo, and M. Vitelli, "Distributed maximum power point tracking of photovoltaic arrays: Novel approach and system analysis," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2610–2621, Jul. 2008.

[4] Y. Xue, K. C. Divya, G. Griepentrog, M. Liviu, S. Suresh, and M. Manjrekar, "Towards next generation photovoltaic inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2467–2474.

[5] [Online]. Available: http://solarbuzz.com/facts-and-figures/retail-price-environment/module-prices

[6] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different dc link configurations," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1320–1333, May 2008.

[7] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[8] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.

[9] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems-an overview," in *Proc. IEEE Int. Symp. Ind. Electron.*, 1998, pp. 224–229.

[10] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[11] *Photovoltaic (PV) Systems—Characteristics of the Utility Interface,* IEC Standard 61727 ed2.0, 2004.

[12] *IEEE Application Guide for IEEE Std 1547, IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems,* IEEE Standard 1547.2-2008, Apr. 2009, pp. 1–207.

[13] *Electromagnetic Compatibility (EMC)—Part 3-2: Limits—Limits for Harmonic Current Emissions (Equipment Input Current Under 16 A Per Phase),* EN 61000-3-2:2006, 2006.

[14] *Automatic Disconnection Device Between a Generator and the Public Low-Voltage Grid,* VDE V 0126-1-1:2006-02, 2006.

[15] P. Mahat, Z. Chen, and B. Bak-Jensen, "Review of islanding detection methods for distributed generation," in *Proc. Int. Conf. Electr. Utility Deregulat. Restruct. Power Technol.*, 2008, pp. 2743–2748.

[16] *Requisitos para la conexión de microgeneradores en paralelo con redes generales de distribución en baja tensión,* UNE-EN 50438:2008, 2008.

[17] T. Kerekes, R. Teodorescu, and U. Borup, "Transformerless photovoltaic inverters connected to the grid," in *Proc. Annu. IEEE Appl. Power Electron. Conf.*, 2007, pp. 1733–1737.

[18] E. Gubía, P. Sanchis, A. Ursúa, J. López, and L. Marroyo, "Ground currents in single-phase transformerless photovoltaic systems," *Progr. Photovoltaics: Res. Appl.*, vol. 15, no. 7, pp. 629–650, Nov. 2007.

[19] S.V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient single-phase transformerless inverters for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3118–3128, Sep. 2010.

[20] B. Sahan, R. Burger, W. Belschner, and N. Henze, "A novel AC module with high-voltage panels in CIS technology," in *Proc. Eur. Photovoltaics Solar Energy Conf. Exhib.*, 2008, pp. 2743–2750.

[21] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "Power decoupling techniques for micro-inverters in PV systems—A review," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 3235–3240.

[22] K. Ogura, T. Nishida, E. Hiraki, M. Nakaoka, and S. Nagai, "Time-sharing boost chopper cascaded dual mode single-phase sinewave inverter for solar photovoltaic power generation system," in *Proc. IEEE Annu. Power Electron. Spec. Conf.*, 2010, pp. 4763–4767.

[23] Y. Kim, J. Kim, Y. Ji, C. Won, and Y. Jung, "Photovoltaic parallel resonant dc-link soft switching inverter using hysteresis current control," in *Proc. Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 2275–2280.

[24] R. West, "Monopolar DC to bipolar DC to AC converter," U.S. 2008/0037305 A1, Feb. 14, 2008.

[25] M. F. Rahman and L. Zhong, "A new, transformerless, photovoltaic array to utility grid interconnection," in *Proc. Int. Conf. Power Electron. Drive Syst.*, 1997, pp. 139–143.

[26] L. Ma, T. Kerekes, R. Teodorescu, X. Jin, D. Floricau, and M. Liserre, "The high efficiency transformer-less PV inverter topologies derived from NPC topology," in *Proc. Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–10.

[27] J. L. Duran-Gomez, E. Garcia-Cervantes, D. R. Lopez-Flores, P. N. Enjeti, and L. Palma, "Analysis and evaluation of a series-combined connected boost and buck-boost dc-dc converter for photovoltaic application," in *Proc. Annu. IEEE Appl. Power Electron. Conf. Exp.*, Mar. 2006, pp. 19–23.

[28] R. Mallwitz, "Circuit apparatus for transformerless conversion of an electric direct voltage into an alternating voltage," U.S. Patent 7.616.467, Nov. 10, 2009.

[29] P. Zacharias and B. Sahan, "Device for feeding electric energy into a power grid and DC converter for such a device," U.S. Patent 8116103 B2, Feb. 14, 2012.

[30] S. V. Araujo, P. Zacharias, and B. Sahan, "Novel grid-connected non-isolated converters for photovoltaic systems with grounded generator," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 58–65.

[31] S. Schoenbauer and F. R. Martin-Lopez, "Single inductor buck boost converter with positive and negative outputs," U.S. Patent 2010/0039080, Feb. 18, 2010.

[32] J.-M. Shen, H.-L. Jou, and J.-C. Wu, "Novel transformerless grid-connected power converter with negative grounding for photovoltaic generation system," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1818–1829, Apr. 2012.

[33] F. Kang, C. Kim, S. Park, and H. Park, "Interface circuit for photovoltaic system based on buck-boost current-source PWM inverter," in *Proc. Annu. Conf. Ind. Electron. Soc.*, 2002, pp. 3257–3261.

[34] S. Saha and V. P. Sundarsingh, "Novel grid-connected photovoltaic inverter," *IEE Proc. Generat., Transmiss. Distrib.*, vol. 143, no. 2, pp. 219–224, Mar. 1996.

[35] O. Abdel-Rahim, M. Orabi, and M. E. Ahmed, "High gain single-stage inverter for photovoltaic AC modules," in *Proc. Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 1961–1967.

[36] Z. Zhao, M. Xu, Q. Chen, J. Lai, and Y. Cho, "Derivation of boost-buck converter based high-efficiency robust PV inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 1479–1484.

[37] Z. Zhao, M. Xu, Q. Chen, J. Lai, and Y. Cho, "Derivation, analysis, and implementation of a boost–buck converter-based high-efficiency PV

inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1304–1313, Mar. 2012.
[38] B. S. Prasad, S. Jain, and V. Agarwal, "Universal single-stage grid-connected inverter," *IEEE Trans. Energy Convers.*, vol. 23, no. 1, pp. 128–137, Mar. 2008.
[39] L. S. Garcia, L. C. de Freitas, G. M. Buiatti, E. A. A. Coelho, V. J. Farias, and L. C. G. Freitas, "Modeling and control of a single-state current source inverter with amplified sinusoidal output voltage," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf.*, 2012, pp. 2024–2031.
[40] L. G. Junior, M. A. G. de Brito, L. P. Sampaio, and C. A. Canesin, "Single stage converters for low power stand-alone and grid-connected PV systems," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2011, pp. 1112–1117.
[41] R. O. Caceres and I. Barbi, "A boost DC–AC converter: Analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134–141, Jan 1999.
[42] T. Liang, J. Shyu, and J. Chen, "A novel DC/AC boost inverter," in *Proc. Intersoc. Energy Convers. Eng. Conf.*, 2004, pp. 629–634.
[43] P. C. Loh, F. Blaabjerg, C. P. Wong, and P. C. Tan, "Tri-state current source inverter with improved dynamic performance," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1631–1640, Jul. 2008.
[44] S. Funabiki, T. Tanaka, and T. Nishi, "A new buck-boost-operation-based sinusoidal inverter circuit," in *Proc. Annu. IEEE Power Electron. Spec. Conf.*, 2002, pp. 1624–1629.
[45] N. Vazquez, J. Almazan, J. Alvarez, C. Aguilar, and J. Arau, "Analysis and experimental study of the buck, boost and buck-boost inverters," in *Proc. Annu. IEEE Power Electron. Spec. Conf.*, 1999, pp. 801–806.
[46] N. Kasa, H. Ogawa, T. Iida, and H. Iwamoto, "A transformer-less inverter using buck-boost type chopper circuit for photovoltaic power system," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, 1999, pp. 653–658.
[47] C. Wang, "A novel single-stage full-bridge buck-boost inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 150–159, Jan. 2004.
[48] S. Jain and V. Agarwal, "A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1928–1940, Sep. 2007.
[49] O. Abdel-Rahim, M. Orabi, and M. E. Ahmed, "Buck-boost interleaved inverter for grid connected Photovoltaic system," in *Proc. IEEE Int. Conf. Power Energy*, 2010, pp. 63–68.
[50] J. C. Yris, H. Calleja, L. Hernández, and J. Olmos, "Design and analysis of a grid-connected inverter without isolation for an AC module," in *Proc. Annu. IEEE Appl. Power Electron. Conf.*, 2012, pp. 2095–2099.
[51] M. Kusakawa, H. Nagayoshi, K. Kamisako, and K. Kurokawa, "Further improvement of a transformerless, voltage-boosting inverter for AC modules," *Solar Energy Mater. Solar Cells*, vol. 67, no. 1–4, pp. 379–387, Mar. 2001.
[52] H. Patel and V. Agarwal, "A single-stage single-phase transformer-less doubly grounded grid-connected PV interface," *IEEE Trans. Energy Convers.*, vol. 24, no. 1, pp. 93–101, Mar. 2009.
[53] P. Zacharias, "Inverter for feeding electric energy into a power supply system," U.S. 2010/0135054 A1, Jun. 3, 2010.
[54] G. Tan, J. Wang, R. Wang, and Y. Ji, "A new SPWM controlled three-switch buck-boost inverter for distributed generation applications," in *Proc. Int. Conf. Power Syst. Technol.*, 2006, pp. 1–6.
[55] B. Hu, L. Chang, and Y. Xue, "Study of a novel buck-boost inverter for photovoltaic systems," in *Proc. Int. Conf. Electr. Mach. Syst.*, 2008, pp. 2602–2606.
[56] Y. Zhang, A. T. Woldegiorgis, and L. Chang, "Design and test of a novel buck-boost inverter with three switching devices," in *Proc. Annu. IEEE Appl. Power Electron. Conf.*, 2012, pp. 1973–1978.
[57] S. Yatsuki, K. Wada, T. Shimizu, H. Takagi, and M. Ito, "A novel AC photovoltaic module system based on the impedance-admittance conversion theory," in *Proc. IEEE Annu. Power Electron. Spec. Conf.*, 2001, pp. 2191–2196.
[58] F. Z. Peng, "Z-source inverter," *IEEE Trans. Power Electron.*, vol. 39, no. 2, pp. 204–510, Mar./Apr. 2003.
[59] Y. Tang, S. Xie, and C. Zhang, "Single-phase Z-source inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3869–3873, Dec. 2011.
[60] D. Cao, S. Jiang, X. Yu, and F. Z. Peng, "Low-cost semi-Z-source inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3514–3523, Dec. 2011.
[61] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, "Generalized multi-cell switched-inductor and switched-capacitor Z-source inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 837–848, Feb. 2013.
[62] R. Gonzalez, J. Coloma, L. Marroyo, J. Lopez, and P. Sanchis, "Single-phase inverter circuit to condition and transform direct current electric power into alternating current electric power," U.S. 2009/0316458 A1, Dec. 24, 2003.
[63] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.
[64] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 693–697, Mar. 2007.
[65] F. Yoneda, "Grid interconnected inverter and grid interconnection device," U.S. 2011/0103117 A1, May 5, 2011.

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